I claim:

1. A semiconductor memory device comprising at least one array of memory cells arranged in rows and columns, means for receiving address information, a selection circuit for selectively accessing at least one of said memory cells in said array, and a plurality of dummy cells arranged along all peripheries of said array, each of said dummy cells having substantially the same configuration as each of said memory cells.

2. The memory device according to claim 1, in which each of said said memory cells and each of said dummy cells include a floating gate type field effect transistor.

3. The memory device according to claim 1, further comprising at least one dummy word line coupled to a part of said dummy cells and means for operatively activating said at least one dummy word line.

4. A semiconductor memory device comprising means receiving address information consisting of N bits (N being a positive integer), an array of memory cells arranged in a matrix form of rows and columns, the number of said memory cells in said array being larger than the 2^N, said memory cells in said array being divided into a

peripheral group and an internal group, the memory cells of said internal group being completely surrounded by the memory cells of said peripheral group, and a selection circuit for selectively accessing at least one of said internal group of memory cells in accordance with said address information.

5. The memory device according to claim 4, in which the number of said internal group of memory cells is 2^N or less.

6. The memory device according to claim 4, further comprising at least one dummy word line coupled to a part of said dummy cells and means for operatively activating said dummy word line.

~~7~~ 3. The memory device according to claim ~~1~~ 1, in which each of said memory cells ~~and each of said dummy cells~~ include a floating gate type field effect transistor.